

Pf-2925/ncc/us/mh

ABSTRACT OF THE DISCLOSURE

A circuit for controlling a cache system having a store queue
5 having plural stages for storing store instructions. The circuit includes : a
first comparator circuit for comparing, in view of index and off-set, an
instruction with tag-retrieval to the store instructions stored in the store
queue ; and a stalling circuit for selectively stalling the instruction with tag-
10 retrieval if the instruction with tag-retrieval corresponds, in view of not
only index but also off-set, to at least one of the store instructions.

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